UPON ACHIEVEMENT OF THE USUAL FUNCTIONS OF TIME WITH PS-3 PLC KLÖCKNER- MOELLER

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ABSTRACT: *This paper shows how to use the PS-3 PLC Klöckner-Moeller, of the programmes for functions of timer used in command installations of electric drives. For the same functions of time, there are several variants of programs using the principle diagrams of electrical and electronic circuits, which carry out the functions of time analyzed, either binary functions corresponding to these circuits. These functions are: the time-on delay, the time-off delay and the time-on and off delays, which are the subject of the paper. Using the program for time-on delay has been achieved the functions of time: the time-off delay and the time-on and off delays. For all the variants, the time-on and off delays is obtained using electrical circuits input with time-off delay or electronic, of an electrical or electronic circuit with the time-on delay.*

In the diagrams of electrical and electronic circuits which perform the functions of time: the time-on delay, the time-off delay and the time-on and off delays, used for the purpose of drawing up appropriate programmes, marking components and signals, is the recognized by PS-3 PLC.

KEYWORDS: *Command installation, PLC, time-off delay, time-on delay.*

1. INTRODUCTION

The paper present programmes shall be established for the main functions of time used for the materialisation, scheduled in logic into electrical command. These functions are: the time-on delay, the time-off delay and the time-on and off delays, which are the subject of the work.

The time-on delay function is using a simple basic program (program no. 1) that is used for the materialization of all the functions of time. For this purpose, PS-3 PLC Klöckner-Moeller has 32 timers TR0 ... TR31. The mean-time timer switches working time in the field of 0.1 s - 6553.5 s [2].

Using this program was made: time-on delay, and in four variants: the time-off delay and the time-on and off delays [1,2,3,4].

For the establishment of programmes in 1st version [1,2], it was left to the rollback using a time-off relay classical installation (fig.2) using conventional electromagnetic relays and a time-on delay relay.

In 2nd and 3rd variants programs, has left from the scheme of the time circuits with time-off delay that have flip-flop RS circuit (CBB-RS) and a time circuit with time-on delay, without (fig.4) and with (fig.6) the command STP (stop time) [1,2].

For the 4th version of the time-off delay program used appropriate circuit with the simplest structure to use in making programs on PLC AP 201 [1,3]. This circuit consists of a circuit with time-on delay, two NOT gates and an OR logic gate (fig.8).

For all programs variants, the time-on and the time-off delay is obtained using electrical circuits with entry delay the return (1st version) or electronic (2nd, 3rd and 4th variants), an electrical or electronic circuit with time-on delay.

In the principle electrical and electronic diagrams which perform the functions of time: the time-on delay, the time-off delay and the time-on and off delays, used for the purpose of drawing up appropriate programmes, marking components and signals, is recognized of PS-3 PLC.

2. THE PROGRAM FOR THE TIME-ON DELAY FUNCTION

As mentioned earlier, this is a basic program that can be used for PS-3 PLC for all time functions. For the timer function has been used TR0. Set the count timer is done with the signal on input I0.0. It not used the STP function, was imposed on the working time t_a at 5s (KW50), the output being Q0.0. It is stated that inputs and outputs can be, also, from internal memory.

During initial time t_0 I0.0 and Q0.0 has 0 logic (fig. 1.c).,

After time t_0, I0.0 = 1 (the logical value 1), but Q0.0 = 0 another time t_a, after that Q0.0=1. After time t_x, I0.0 = 0 and Q0.0 = 0. The times t_x and t_y are the time

intervals in which the signals I0.0 and Q0.0 have logical value 1. The relationship between the t_y and t_x is:

$$t_y = t_x - t_a \quad (1)$$

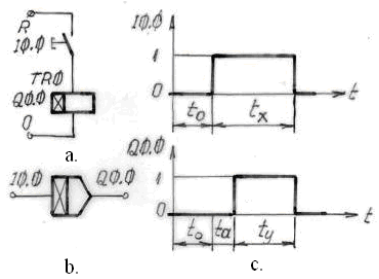

Fig. 1. Realization of time-on delay function: a. The function scheme using a classic time-on delay relay; b. The block diagram of an electronic circuit time-on delay; c. Variations in time of input signals (I0.0 = $f_1(t)$) and output (Q0.0 = $f_2(t)$)

Program no. 1
Time-on delay

```
000 TR0
    TR0 * S : I0.0
    TR0 * STP :
    TR0 * IW : KW50
    TR0 * EQ : Q0.0
```

3. PROGRAMMES FOR THE TIME-OFF DELAY AND TIME-ON AND OFF DELAYS, 1ST VARIANT

3.1. Time-off delay, 1st variant

Program was made using installation command given in fig.2a. When action the button I0.1 the normally open switch (n.o.s.) is close, I0.1 from circuit 1 and is open the normally close switch (n.c.s.) I0.1 from circuit 3. Close the relay Q0.1 because his coil shall be supplied with the voltage source through n.o.s. I0.1 and open time normally close switch (o.t.n.c.s.) M0.1 from circuit 1, so when signal I0.1 increase to the 1 logic value, after initial time t_0 and the signal Q0.1 increases from 0 to 1 logic (fig.2.d).

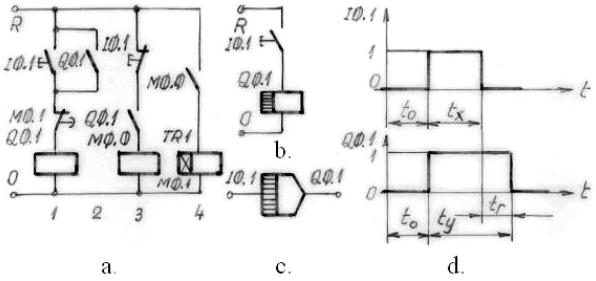

Fig. 2. Realization of time-off delay function, 1st variant; a. The principle scheme of the installation command performs the function; b. The classical equivalent schemes; c. The electronic circuit; d. Variations in the time of the signal input (I0.1 = $f_1(t)$) and output (Q0.1 = $f_2(t)$)

Program no. 2
Tim-off delay, 1st variant

```
001 L I0.1
002 O Q0.1
003 A NM0.1
004 = Q0.1
005 L NI0.1
006 A Q0.1
007 = M0.0
008 TR1
    TR1 * S : M0.0
    TR1 * STP :
    TR1 * IW : KW35
    TR1 * EQ : M0.1
```

Close n.o.s. Q0.1 from circuit 2, that short-circuit n.o.s. I0.1, from circuits 1 and 3 in preparing the power supply voltage of the relay's coil M0.0. The button I0.1 is actions a time t_x, I0.1 remains at 1 logic level. After this time the input signal passes from the 1 logical value to 0 value logic. Opens n.o.s. I0.1 from circuit 1 and closes n.c.s. I0.1 from circuit 3. The relay coil of Q0.1 remains supplies with voltage through n.o.s. Q0.1, from circuit 2 and o.t.n.c.s M0.1 from circuit 1. By closing of n.c.s. I0.1 from circuit 3 is supplied with voltage the relay coil M0.0. Closes n.o.s M0.0 from circuit 4 and supplies with voltage the time relay coil TR1 (M0.1) with the time-on relay, which after adjusted time t_a acting on o.t.n.c.s. M0.1 from circuit 1, which it opens.

If supply voltage is switch off on the coil and open n.o.s. Q0.1 from the circuits 2 and 3. Through opening n.o.s. from circuit 2 saving the 0 logical value of the output signal (Q0.1 = 0), and n.o.s. Q0.1 from circuit 3 interrupt the voltage supply to relay's coil M0.0; opens n.o.s. M0.0 from circuit 4, interrupt the voltage supply of time relay TR1 (M0.1) and closed the o.t.n.c.s. M0.1 preparing the installation for a new operating cycle. In conclusion the signal on the input I0.1 has 1 logical value a time t_x and on the output Q 0.1, a longer time t_y (fig. 2 d):

$$t_y = t_x + t_r \quad (2)$$

the difference between the two periods of time being the return time delay t_r of the equivalent time-off relay with the electrical diagram presents in fig. 2.b, so:

$$t_r\,(Q0.1) = t_a\,(TR1, M0.1) \quad (3)$$

For command installation (fig.2.a) logical functions are:

$$Q0.1 = (I0.1 + Q0.1)\cdot \overline{M0.1}(t_a) \quad (4)$$

$$M0.0 = \overline{I0.1}\cdot Q0.1 \quad (5)$$

$$M0.1(t_a) = M0.0 \quad (6)$$

With these functions or with the principle of the scheme from fig. 2 was made time-off delay has been program no. 2: the time-off delay, 1st variant: lines 001…004 materializes circuits 1 and 2, respectively a logical function (4), 005...007 lines, the circuit 3 (function (5)), and the line 008 the 4 circuit (function (6)).

3.2. Time-on and off delays, 1st variant

To carry out this function at the input of the command installation that materializes the time-off delaying function, 1st variant (fig.2.a) shall be fitted with a time-on relay with the working time t_{a1}. Operation of this installation is the same as the previous analysis that differs in that instead of the button I0.1 it use contacts M0.2, from circuits 2 and 4 with delayed closing and opening.

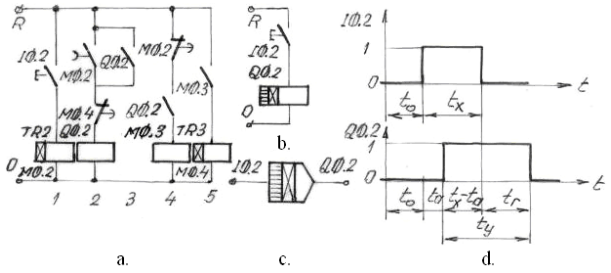

Fig. 3. Realization of the function of the time-on and off delays, 1st variant: a. The principle scheme of the installation command that performs the function of time; b. and c. Classical equivalent schemes (b) and electronic circuit (c); d. Variations in the time of the input signals (I0.2 = $f_1(t)$) and output (Q0.2 = $f_2(t)$)

Program no. 3
Time-on and off delay, 1st variant

```
009  TR2
     TR2 * S : I0.2
     TR2 * STP :
     TR2 * IW : KW30
     TR2 * EQ : M0.2
010  L M0.2
011  O Q0.2
012 A NM0.4
013 = Q0.2
014 L NM0.2
015 A Q0.2
016 = M0.3
017 TR3
     TR3 * S : M0.3
     TR3 * STP :
     TR * IW : KW60
     TR3 * EQ : M0.4
```

Analyzing the operation of the command installation (fig.3.a), it appears that the press button I0.2, the relay Q0.2 the relay does not act until after the working time t_{a1} ($t_{a1} = t_a$) of time TR2 (M0.2), and in return n.o.s. I0.2, the relay Q0.2, remains driven a while t_{a2} ($t_{a2} = t_r$), which is the working time of the second time relay (TR3(M0.4)).

Dependence between the length t_y of the signal output Q0.2 and the length t_x signal input of I0.2, the time periods in which these signals are logic 1, is given by (fig.3.d):

$$t_y = t_x - t_a + t_r \qquad (7)$$

Further are given the logical functions for installation from fig.3.a:

$$M0.2(t_{a1}) = I0.2; \qquad (8)$$

$$Q0.2 = (M0.2(t_{a1}) + Q0.2) \cdot \overline{M0.4(t_{a2})}; \qquad (9)$$

$$M0.3 = \overline{M0.2(t_{a1})} \cdot Q0.2; \qquad (10)$$

$$M0.4(t_{a2}) = M0.3. \qquad (11)$$

Using the principle of the scheme from fig. 3.a or logical functions corresponding to the command installation, was made the no. 3 program, who materializes on the PS-3 PLC time-on and off delays, as follows: with line 009 is the circuit 1 from fig.3.a, respectively (function (8)); with lines 010... 013 circuits 2 and 3 (function (9)); with 014… 016 lines circuit 4 (function (10)), and with the line 017, circuit 5 (function (11)).

3.3. Programmes for the time-off and time on and off delays functions, 2nd variant

3.3.1. Time-off delay, 2nd variant

Electronic circuit which makes the time-off relay, 2nd variant, has in its composition, as basic elements, a RS flip-flop circuit and a time-on delay circuit (fig. 4).

Representation in block diagrams and signals diagrams of the input (I0.3) and output (Q0.3) are those shown in fig.2.c and d, the only place I0.1 and Q0.1 signals is taken I0.3 and Q0.3.

When the input signal I0.3 increases from 0 logical value to value 1, S = 1; because initial the R = 0, results Q = 1, so at the output of CBB-RS the signal Q0.3 = 1. After the NOT1 gate the signal circuit has 0 logical value which locks the AND 2 gate.

This state lasts a while t_x (fig.2.d) after which I0.3 = 0, when S = 0 and R = 0, but Q0.3, remains at the previous logical value (Q0.3 = 1). Now at the output circuit 1 $\overline{I0.3}$ = 1, the AND gate is open and M0.5 = 1. The time-on delay circuit TR4 is turned on, that after working time t_a (t_a = 6 s) determines M0.6 = 1 (R = 1) and Q0.3=0. The duration t_a is the relay time-off delay (t_r).

Using the principle of electronic time-off delay circuit, 2nd variant, from fig. 4, there has been no.4 program, on PS-3 PLC. To do this, must need to define the signals S and R inputs of CBB-RS. On the S input applies the signal I0.3, and on R input, the signal M0.6, which is obtained with the program's first four lines (018…021). The last four lines (022…025) carries out the RS flip-flop circuit (CBB-RS).

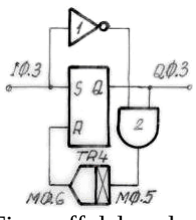

Fig. 4. Time-off delay electronic circuit, 2nd variant

Program no. 4
Time-off delay,2nd variant

```
018 L NI0.3
019 A Q0.3
020 = M0.5
021 TR4
      TR4 * S : M0.5
      TR4 * STP :
      TR4 * IW : KW60
      TR4 * EQ : M0.6
022 L I0.3
023 S Q0.3
024 L M0.6
025 R Q0.3
```

3.3.2. Time-on and off delays, 2nd variant

Electronic time circuit configuration with time-on and off delays, 2nd version, is obtained by fitting the electronic circuit on the entry of time-off delay, 2nd variant (fig.4) of an electronic time circuit with the time-on delay (TR5, fig.5).

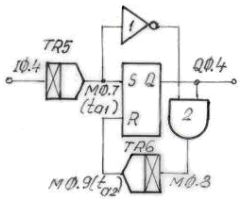

Fig. 5. Electronic time circuit with time-on and off delays, 2nd variant

In its original state signals I0.4, M0.8 and M0.9 have the logical value 0.

When the input signal I0.4 increases from 1 logical value after working time t_{a1} ($t_{a1} = t_a$), at the output of time circuit TR5, M0.7 move from the logical value 1 to 0. Because on the CBB inputs S = 1 and R = 0, Q = 1 and Q0.4=1. When I0.4 switch from logical value 1 to value 0, M0.7 = 0, S = 0, R = 0, but Q and Q0.4 remain at logical value 1. After NOT1 gate the signal has the value 1, because Q0.4 = 1, at the output AND2 gate M0.8 = 1 and is activated the time circuit with time-on delay TR6 with working time t_{a2} ($t_a = t_r$). After the time t_{a2} signal M0.9=1 of the output circuit TR6. On the CBB -RS inputs, S = 0, R = 1, so Q0.4 = 0.

This electronic time circuit it symbolizes as shown in fig.3.c, and variations in the time of the signals input and output are the same as in fig.3.d, only I0.2 and Q0.2 signals are taken by I0.4 and Q0.4.

Using fig. 5 has been made program no.5 which materializes on the PS-3 PLC electronic time circuit with time-on and off delays, 2nd version.

It is necessary in this case, the definition of inputs S and R of CBB-RS (M0.7 (t_{a1})) and (M0.9 (t_{a2})). With the first line of the program (026) is M0.7 (t_{a1}), and with (027 .... 030) results M0.9 (t_{a2}). With the latest program lines (031...034) is the CBB-RS.

Program no. 5
Time-on and off delays, 2nd variant

```
026 TR5
      TR5 * S : I0.4
      TR5 * STP :
      TR5 * IW : KW30
      TR5 * EQ : M0.7
027 L NM0.7
028 A Q0.4
029 =  M0.8
030 TR6
      TR6 * S : M0.8
      TR6 * STP :
      TR6 * IW : KW60
      TR6 * EQ : M0.9
031 L M0.7
032 S Q0.4
033 L M0.9
034 R Q0.4
```

3.4. Programmes for the time-off and time on and off delays functions, 3rd variant

3.4.1. Time-off delay, 3rd variant

In 3rd variant the time-off delay is made using only two circuits, a CBB-RS and a timer control with STP control (stop timing), as shown in fig. 6.

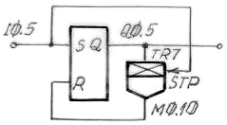

Fig.6. Electronic time circuit with time-off delay, 3rd version

In its original state the signals I0.5 and Q0.5 and M0.10 have logical value 0, so inputs on CBB-RS: R = 0 (I0.5 = 0) and S = 0 (M0.10 = 0), and the Q = 0 (Q0.5 = 0). When the input signal I0.5 passes from logical value 0 to value 1, S = 1, R = 0, so Q0.5 = 1. The input signal I0.5 has a logic value of 1, and locks timer operation TR7.

Changing the value of the signal I0.5 (I0.5 = 0), the time circuit TR7 is activated and after the time required (6 s) M0.10=1 (signal output from the timer). Now S = 0 (I0.5 = 0) and R = 1 (M0.10 = 1), results Q = 0, so Q 0.5 = 0.

With the principle of electronic circuit time delay, with time-off delay, 3rd variant, has been made the program no. 6 on PS-3 PLC. The first program line (line 035) is time-on delay circuit TR7 containing the command STP, unlike previous programs. The working time t_a (t_a = 6 s) of the timer TR7, is the remain time t_r of the time circuit from fig. 6.

Dependencies of input signals (I0.5) and output (Q 0.5) depending on the time of this circuit and block diagram, are like the time-off delay circuit analyzed so far.

Program no. 6
Time-off delay, 3rd variant

```
035 TR7
      TR7 * S : Q0.5
      TR7 * STP : I0.5
      TR7 * IW : KW60
      TR7 * EQ : M0.10
036 L I0.5
037 S Q0.5
038 L M0.10
039 R Q0.5
```

3.4.2. Time-on and off delays, 3rd variant

This time circuit based on the structure of electronic circuit with the time-off delay (fig. 6) on the input is fitted with a time-on delay.

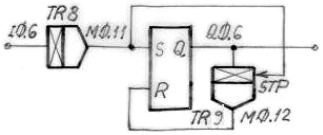

Fig. 7. Electronic time circuit with time-on and off delays, 3rd variant

Variations in the time of the input signal (I0.6) and output (Q0.6) and block diagram of this circuit are identical to those of the time-on and off delays presented earlier.

In original condition all variables from the principle scheme of the electronic circuit, have the logical value 0.

After an initial period of time t_0 the signal I0.6 = 1 is activated timer TR8 and after the time t_{a1} ($t_{a1} = t_a$) required by the programme, the signal M0.11 from the output of this circuit has the logical value 1. In this state S = 1 (M0.11 = 1) and R = 0 (M0.12 = 0), so at the output CBB-RS, Q = 1, (Q0.6 = 0). TR9 timer is blocked by M0.11 = 1.

When changing the value, from 1 to 0 the signal logic I0.6 (M0.11 = 0), so S = 0 and R = 0 (M0.12= 0) a time t_{a2} ($t_{a2} = t_r$) enforced by the timer TR9 (through program). Because the signal of M0.11 that locks TR9 circuit, has logical value 0, activates the timer. It was shown that during the t_{a2} S = 0 and R = 0, and Q0.6 remains at the previous logical value (Q0.6 = 1). After the time t_{a2}, M0.12 = 1, so R = 1. Now R = 1 and S = 0, so Q0.6 = 0.

With the help of the principle scheme design of the electronic time circuit with time-on and off delays, 3rd version has been made program no. 7 on PS-3 PLC. It have defined input signals S (M0.11) and R (M0.12) of CBB-RS that setting the program lines 040 and 041, after which, with the last four lines (042...045) the CBB-RS.

Program no. 7
Time-on and off delays, 3rd variant

```
040  TR8
     TR8 * S : I0.6
     TR8 * STP :
     TR8 * IW : KW30
     TR8 * EQ : M0.11
041  TR9
     TR9 * S : Q0.6
     TR9 * STP : M0.11
     TR9 * IW : KW60
     TR9 * EQ : M0.12
042  L M0.11
043  S Q0.6
044  L M0.12
045  R Q0.6
```

3.5. Programmes for the time-off and time on and off delays functions, 4th variant

3.5.1. Time-on delay, 4th variant

Electronic time circuit with time-off delay, in this variant (fig.8) consists of the basic element, TR0 timer, NOT2 and NOT3 gates and OR 1 gate.

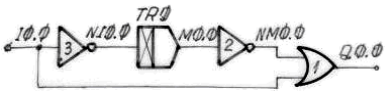

Fig.8. Electronic time circuit with time-off delay, 4th version

In the initial state input signal I0.0 has the value logical 0, after NOT3 gate signal has the value 1. During time t_a of TR0 timer, signal M0.0 = 0, so at the output NOT2 gate NM0.0 = 1. Results that Q0.0 = 1, during time t_a, after which M0.0 = 1, NM0.0 = 0, since the signal on the second input of OR1 gate has the value 0, as a result of Q0.0 = 0. When I0.0 = 1, since this applies to the second input of OR1 gate, results that output signal Q0.0 becomes 1.

After NOT3 gate, NI0.0 = 0, and after NOT2 gate, NM0.0 = 1, the following two inputs of the OR1 gate, the signals have logical value 1 (Q0.0 = 1). The return signal I0.0 at the logical value 0, on the second input of the OR1 gate the signal has the value 0, but on the first logical input signal NM0.0 = 1 on the working time t_a ($t_r = t_a$) of timer TR0. After this time and signal NM0.0 = 0, so, the electronic time circuit with time-off delay, 4th variant, Q0.0 = 0.

Program no. 8
Time-off delay, 4th variant

```
000 TR0
    TR0 * S : NI0.0
    TR0 * STP :
    TR0 * IW : KW60
    TR0 * EQ : M0.0
001 L NM0.0
002 O I0.0
003 = Q0.0
```

3.5.2. Time-on and off delays, 4th variant

And in this case, the electronic time circuit, with time-on and off delays is obtained by fitting the input delay time circuit with time-off delay (TR1, fig. 9).

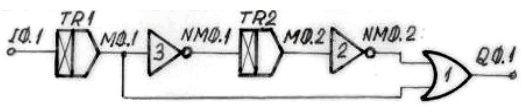

Fig. 9. Electronic time circuit with time-on and off delays, 4th variant

When the voltage supply of the electronic circuit, the circuit signals time have values: I0.1 = 0, M0.1 = 0, NM0.1 = 1, M0.2 = 0, a time t_{a2} ($t_r = t_{a2}$), which is the working time of TR2 timer, NM0.2 = 1, so Q0.1 = 1.

After the time t_{a2} ($t_{a2} < t_0$) signals I0.1, M0.1 and NM0.1 remain at previous logical values, and the other,

changes the logical values (M0.2 = 1, NM0.2 = 0, and Q0.1 = 0). This is the initial state of an electronic circuit with time-on and off delays, 4th version. The time t = t_0, I0.1 = 1, but other signals remain to the previous logical values during working time t_{a1} ($t_a = t_{a1}$) of timer TR1.

After this time interval M0.1= 1, so Q0.1 =1, NM0.1 = = 0, M0.2=0 and NM0.2 = 1 (Q0.1 = 1). This state is maintained throughout the I0.1 = 1. When I0.1 = 0 results M0.1 = 0, NM0.1 = 1, but M0.2 = 0 during the time t_{a2} ($t_r=t_{a2}$) NM 0.2 = 1, and as a result and Q0.1 = 1. After the time t_{a2}, M0.2 = 1, NM0.2 = 0; because M0.1 = 0 and the output OR1 gate the signal Q 0.1 = 0. Using the principle of electronic time circuit with time-on and off delays, 4th version, given in fig. 9, has been made the program no. 9 on PS-3 PLC.

Program no. 9
Time-on and off delays, 4th variant

```
004  TR1
     TR1 * S : I0.1
     TR1 * STP :
     TR1 * IW : KW30
     TR1 * EQ : M0.1
005 TR2
     TR2 * S : NM0.1
     TR2 * STP :
     TR2 * IW : KW60
     TR2 * EQ : M0.2
006 L NM0.2
007 O M0.1
008 = Q0.1
```

4. CONCLUSIONS

In this work has been presented in detail, the way of the four variants of realization of circuits with time-off delay and time-on and off delays. Obviously, the simple programs are 3rd and 4th variants of electronic circuits of proper time.

Electronic circuits, the 4th version, has the disadvantage that the power supply voltage, with a duration of time t_a, how is working time of the timer electronic circuit with time-off delay, the output signals has the value logic 1. That is why it is essential that the initial time $t_0 > t_a$. For use in command installations of these circuits or programs is necessary first to supply the installation, in wired logic or program (PLCs), and after a while $\Delta t = t_0 - t_a$, is put under the voltage the installation.

Analyzing the four variants of the materialisation of time functions: the time-on and time-on and off delays, it follows that the 3rd version of the electronic circuit (fig. 6 and 7) and their related programs (the programs no. 6 and 7), it is recommended to be used in custom made installations in wired logic or program (with PLCs).

The work has a pronounced didactic character, but the programmes submitted, can be used not only to solving the draft projects, or dissertation which include programs on PLCs, but also to help those who use industrial PS-3 PLCs, Klöckner-Moeller, as well as other types of PLCs (older version).

5. REFERENCES

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